

Application No.: 10/776,228

Docket No.: 2336-241

**REMARKS**

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 2-21 are pending in the application. Claims 6, 8 and 11 have been amended to better define the claimed invention. Amended independent claims 8 and 11 find solid support in the original specification, e.g., at page 15, lines 20-23 and page 17, lines 11-17. No new matter has been introduced through the foregoing amendments.

The 35 U.S.C. 103(a) rejection of claims 2-21 as being obvious over *Orita* in view of *Toshiba* and *Lee* is traversed for the reasons advanced in the un-entered after-final Amendment filed November 23, 2005, at pages 7-9, which are incorporated herein by reference.

Solely for the purpose of expediting prosecution, Applicants have further amended the independent claims to specifically define the invention over the art.

In particular, amended independent claims 8 and 11 additionally recite that the nitride semiconductor crystal film is 'un-doped' nitride. Therefore, the additional heat treatment process (the step (c') of claim 8 or (d) in claim 11) is performed on the 'un-doped' nitride semiconductor crystal film, after performing a surface treatment process and before forming the first conductive nitride semiconductor layer.

However, the cited references (particularly *Orita* and *Toshiba*) fail to disclose, teach or suggest an additional heat treatment process performed on a un-doped nitride film.

The *Toshiba* annealing process is performed on the p-type GaN layer and n-type GaN layer to activate the p-type dopant and prevent deterioration of the n-type GaN layer. See *Toshiba*

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at Abstract and paragraphs [0009] and [0020]. Thus, *Toshiba* annealing process is performed on doped layers, rather than a un-doped layer as presently claimed.

The Examiner's allegation in the Advisory Action that the additional heat treatment is taught by *Orita* at column 3, lines 39-53 is noted. This allegation seems to contradict the Examiner's previous holding that *Orita* does not teach or suggest such additional heat treatment. See the first Office Action dated February 09, 2005 at page 4, line 1 of, and the Final Office Action dated August 23, 2005 at page 3, line 3. The Examiner is kindly asked to set forth a consistent position, so that his rejection(s) can be properly understood and responded to.

In addition, *Orita*, at column 3, lines 39-53 as cited in the Advisory Action, does not teach or suggest any heat treatment. It appears to be the Examiner's intent to cite column 4, lines 39-53 instead. If so, Applicants respectfully submit that *Orita* does not teach or suggest the claimed additional heat treatment at column 4, lines 39-53. The reference only discloses a surface treatment for removing an oxide film on the first semiconductor layer 12, rather than an additional heat treatment process performed on the un-doped nitride semiconductor crystal film as presently claimed. See *Orita* at column 4 lines 24-28 and 39-53. *Orita* also fails to teach or suggest that the first semiconductor layer 12 is un-doped.

Accordingly, Applicants respectfully submit that all claims in the present application are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such

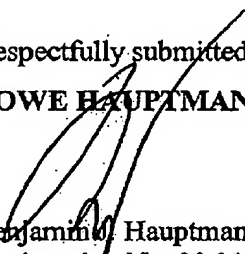
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deposit account.


Respectfully submitted,

**LOWE HAUPTMAN & BERNER, LLP**

  
Benjamin Hauptman  
Registration No. 29,310

USPTO Customer No. 22429  
1700 Diagonal Road, Suite 310  
Alexandria, VA 22314  
(703) 684-1111 BJH/KL/klb  
(703) 518-5499 Facsimile  
Date: January 23, 2006

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